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REMARKS/ARGUMENTS

Reconsideration of the present application, as amended, is respectfully requested.

The June 20, 2006 Office Action and the Examiner's comments have been carefully considered. In response, claims are cancelled and amended and remarks are set forth below in a sincere effort to place the present application in form for allowance. The amendments are supported by the application as originally filed. Therefore, no new matter is added.

PRIOR ART REJECTIONS

In the Office Action claims 1-3, 5-9, 11, 12 and 14-18 are rejected under 35 USC 103(a) as being unpatentable over USP 5,510,807 (Lee et al.) in view of USP 5,825,343 (Moon), and further in view of USP 5,561,381 (Jenkins et al.). Claims 10 and 19 are rejected under 35 USC 103 as being unpatentable over Lee et al. in view of Moon and Jenkins et al., and further in view of USP 6,825,823 (Taira et al.).

In the liquid crystal display device and drive control method respectively recited in amended claims 1 and 12, in at least one signal application period set in a field period, an initialization signal voltage is applied to a signal line, and a first gate pulse is supplied to a scanning line, thereby applying

an initialization signal voltage to a display pixel. Then, after application of the initialization signal voltage to each signal line ends, and a predetermined hold time lapses, a display signal is supplied to the signal line, and a second gate pulse is supplied to the scanning line, thereby supplying a display signal to the display pixel.

The hold time is set to be equal to or longer than a voltage-write response time of the display pixels, and the value of the initialization signal voltage is set to be equal to or higher than the maximum voltage value of the display signal, whereby the liquid crystal capacitances just after supply of the second gate pulse are necessarily substantially constant without depending on the value of the display signal. As a result, the amount of voltage change of the pixel electrode just after supply of the second gate pulse ends is substantially constant without depending on the value of the display signal. Thus, the voltage change of the pixel electrode can be easily canceled by adjusting, e.g., adjusting the common electrode voltage, and a satisfactory display quality can be obtained.

In contrast, Lee et al. teach a structure in which in a selection period in which a scanning signal is supplied to a scanning line, after a precharge pulse is supplied to each data line, VIDEO DATA is successively supplied to each block of a data

line. In Lee et al., supply of the precharge pulse and VIDEO DATA is continuously carried out in the selection period in which the scanning signal is supplied.

In the present claimed invention, however, the initialization signal and the display signal are respectively supplied in association with the first and second gate pulses which are separately applied. Thus, the initialization signal voltage and display signal of the present claimed invention are different from the precharge pulse and VIDEO DATA of Lee et al.

Furthermore, the voltage value of the precharge pulse of Lee et al., as shown in FIG. 6, is set such that a precharge pulse V^+, which is positive-going for odd-number data lines, is set to a value which is close to and lower than the maximum value 5V, and a precharge pulse V^-, which is negative-going for even-number data lines, is set to a value which is close to and higher than the minimum value 0. In an application period of the VIDEO DATA, charging is carried out until the precharge pulse reaches the maximum voltage 5V or the minimum voltage 0V. On the other hand, in the present claimed invention, the value of the initialization signal voltage is set to be equal to or higher than the maximum voltage value of the display signal, as a result of which the liquid crystal capacitances just after supply of the second gate pulse are necessarily constant without depending on the value of

the display signal. This structural feature is different from that taught in Lee et al.

Moon discloses a structure in which a gate pulse is supplied to a gate line two times at intervals of 1H, and the liquid crystal capacitor is pre-charged by the first gate pulse. That is, in Moon, as shown in Fig.8 thereof, the time interval between supply of one of two gate pulses and that of the other is 1H, and is set in accordance with the supply timing of a gate pulse to another gate line.

In contrast, in the present claimed invention, the time interval between the first and second gate pulses is set at a predetermined hold time, which is set to be equal to or longer than the voltage-write response time. Therefore, two gate pulses supplied to a single gate line in Moon are different from the first and second gate pulses of the present claimed invention.

Furthermore, even if Moon is combined with Lee et al., the structural features set forth in amended claims 1 and 12 cannot be derived from such a combination, since neither Lee et al. nor Moon discloses, teaches or suggests that two gate pulses are applied to a scanning line at an interval set to be equal to or longer than the voltage-write response time of the liquid crystal of the display pixels.

Jenkins et al. disclose the structure of a sense circuit for detecting charge on a TFT/LCD cell capacitor, to test TFT and LCD cell arrays prior to assembly of a liquid crystal panel. FIG. 5 of Jenkins et al. shows a timing diagram for a test by the sense circuit. In FIG. 5, T4 to T8 denote hold time periods. Each of the hold time periods is a time period in which an actual display accumulates charge is emulated. The structure of Jenkins et al. is a structure for testing whether a TFT/LCD cell is good or bad. That is, it does not suggest the operation timing of displaying an actual image. Furthermore, in FIG. 5 of Jenkins et al., T4 to T8 denote time periods in each of which the actual display is emulated. However, this corresponds to an ordinary driving method in which a gate pulse is supplied to a scanning line once; that is, it does not correspond to a structure in which two gate pulses, i.e., first and second gate pulses, are supplied to a single scanning line as recited in the present claimed invention.

Therefore, even if Lee et al., Moon and Jenkins et al. are combined together, such a combination does not disclose, teach or suggest the structure of the present claimed invention.

In view of the foregoing, independent claims 1 and 12 are patentable over all of the references of record under 35 USC 102 as well as 35 USC 103.

Dependent claims 2, 3, 5-9, 11 and 14-18 are either directly or indirectly dependent on claims 1 and 12 and are patentable over the cited references in view of their dependence on claims 1 and 12 and because the references do not disclose, teach or suggest each of the limitations set forth in the dependent claims.

With regard to the rejection of claims 10 and 19, these claims are dependent on claims 1 and 12 respectively, and are patentable over the cited references in view of their dependence on claims 1 and 12.

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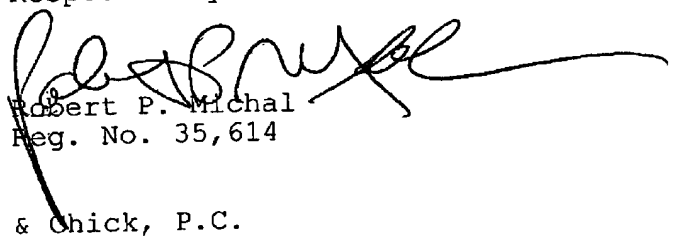
Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner disagrees with any of the foregoing, the Examiner is respectfully requested to point out where there is support for a contrary view.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,



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Encl.: Petition for Extension of Time